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EXAMINER	
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ART UNIT	**PAPER NUMBER**
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8

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,841	HEITKAMP ET AL.	
	Examiner	Art Unit	
	Khanh Dang	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3 and 5-29* is/are rejected.

7)☒ Claim(s) *2 and 4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

Claims 21, 22, and 26 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With regard to claims 21 and 22, the essential structural cooperative relationships between elements recited in claim have been omitted, such omission amounting to a gap between the necessary structural connections. MPEP 2171.02.

With regard to claim 26, the essential structural cooperative relationships between the means plus functions recited in claim have been omitted, such omission amounting to a gap between the necessary structural connections. MPEP 2171.02.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the

United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3, 5-9, 11-18, and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Khosrowpour et al.

It is first noted that similar claims will be grouped together to avoid repetition in explanation.

As broadly drafted, these claims do not define any structure that differs from Khosrowpour et al. With regard to claims 1, 5, 6, 7, 8, 11, 12, 13, 14, 15, and 26, Khosrowpour et al. discloses a control system, comprising: a bus (104); a master device (102) connected to the bus and configured to commence a bus cycle that includes an address interval and a data interval, provide a destination address on the bus during the address interval, and transmit or receive a command or data during the data interval; and a plurality of slave devices connected to the bus and configured to detect commencement of the bus cycle, begin to sample the destination address from the bus a plurality of clock cycles after commencement of the address interval, and transmit or receive a command or data during the data interval. Note that SMB (104) employs I2C Bus. I2C is a 2-wire serial interface standard defined by Philips Semiconductor. The I2C Bus physically consists of 2 active wires and a ground connection. The active wires, SDA and SCL, are both bi-directional. SDA is the Serial Data line and SCL is the Serial Clock line. The I2C interface is a master/slave type interface. Only two lines (clock and data) are required for full duplexed communication between multiple devices. With I2C, each IC on the bus has a unique address. A device that controls signal transfers on the

line in addition to controlling the clock frequency is the master and a device that is controlled by the master is the slave. The master can transmit or receive signals to or from a slave, respectively, or control signal transfers between two slaves, where one is the transmitter and the other is the receiver. I2C bus support more than one master connected to one bus. It is possible to combine several masters, in addition to several slaves, onto an I²C-bus to form a multi-master system. To begin communication, the bus master places the address of the device with which it intends to communicate (the slave) on the bus. All ICs monitor the bus to determine if the master device is sending their address. Only the device with the correct address communicates with the master. I2C Specification is readily available at Philips Semiconductor. Also see at least claim 1; Figs. 1, 1A, and 2 and description thereof). With regard to claim 3, see above and Fig. 1A and description thereof. With regard to claim 9, the sample circuit of Khosrowpour et al. resamples data bit after the reset of the control logic after a predetermined time. With regard to claim 16, since the system of Khosrowpour et al. is a server-type and can be controlled remotely it can be said that such a system is a "network device." With regard to claims 17 and 18, one using the system of Khosrowpour et al. would have performed the same steps set forth in claims 17 and 18.

Claims 23, 24, and 27-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Dickson et al.

It is first noted that similar claims will be grouped together to avoid repetition in explanation.

As broadly drafted, these claims, after the word "comprising," do not define any structure that differs from Dickson et al. With regard to claims 23, 24, 27-29, Dickson et al. discloses a network device, comprising: a plurality of redundant buses (bus shown in Fig. 1 for providing connection between 17 and 24 via 18, not labeled, perpendicular to bus 20, bus 20); a plurality of redundant master controllers (18, 19) connected to corresponding ones of the buses (bus shown in Fig. 1 for providing connection between 17 and 24 via 18, not labeled, perpendicular to bus 20, bus 20), one of the master controllers being an active master and other ones of the master controllers being standby masters, the active master being configured to commence a bus cycle that includes an address interval and a data interval, provide a destination address on the corresponding bus during the address interval, and transmit or receive a command or data during the data interval; and a plurality of slave controllers (peripheral device controllers, see also col. 2, lines 34-37) connected to the bus and configured to detect commencement of the bus cycle, sample the destination address from the bus a predetermined amount of time after commencement of the address interval, and transmit or receive a command or data during the data interval. See at least Figs. 1-4 and description thereof.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 10, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khosrowpour et al.

Khosrowpour et al., as discussed above, disclsose the claimed invention except the use of a "5 clock cycles." It would have been obvious to one of ordinary skill in the art at the time the invention was made to use "5 clock cycle" in Khosrowpour et al., since using a particular number of cycles is an obvious design choice; and only involves routine skill in the art. In any event, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dickson et al.

Dickson et al., as discussed above, discloses the claimed invention except the use of master controllers as "router" and slave controllers as "switching and forwarding modules." It would have been obvious to one of ordinary skill in the art at the time the

invention was made to use the system of Dickson et al. in a network environment (note that every network includes routers and switches), since it has been held that the manner in which a claimed apparatus is intended to be employed (in a network environment) does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. *Ex parte Masham*, 2 USPQ2d 1647 (1987).

Response to Arguments

Applicants' arguments filed 2/25/2004 have been fully considered but they are not persuasive.

At the outset, Applicants are reminded that claims subject to examination will be given their broadest reasonable interpretation consistent with the specification. *In re Morris, 127 F.3d 1048, 1054-55 (Fed. Cir. 1997)*. In fact, the "examiner has the duty of police claim language by giving it the broadest reasonable interpretation." *Springs Window Fashions LP v. Novo Industries, L.P.*, 65 USPQ2d 1862, 1830, (Fed. Cir. 2003). Applicants are also reminded that claimed subject matter not the specification, is the measure of the invention. Disclosure contained in the specification cannot be read into the claims for the purpose of avoiding the prior art. *In re Sporck*, 55 CCPA 743, 386 F.2d, 155 USPQ 687 (1986).

With this in mind, the discussion will focus on how the terms and relationships thereof in the claims are met by the references. Response to any limitations that are not

in the claims or any arguments that are irrelevant and/or do not relate to any specific claim language will not be warranted.

The 112, 2nd Paragraph Rejection:

With regard to claims 21 and 22, these claims stand rejected under 35 U.S.C. 112, 2nd paragraph as set forth in a previous Office Action. Claims 21 and 22 are only allowable if rewritten or amended to overcome the 112 Rejection.

With regard to claim 26, Applicants argued that the "system also include several means-plus-function elements that perform an operation 'on the bus.'" Applicants also amended claim 26 to recite that each of the recited means is connected to the bus. In response, the Examiner maintains the 112 rejection of claim 26. Claim 26 is an apparatus claim claiming a plurality of different means. However, the essential structural cooperative relationships between these "means" have been omitted, such omission amounting to a gap between the necessary structural connections. MPEP 2171.02. As disclosed, the master commences a bus cycle and provides destination address and data, and the slave samples the address and data. Therefore, it is not ascertained what may be the difference between the plurality of "means" as claimed in claim 26. For example, it is not ascertained what may be the difference between the "master disclosed in the specification and "means" (line 1 of claim 26), "means" (line 3), and "means" (line 8), as claimed in claim 26. If the plurality of "means" in claim 26 is in fact distinct elements, Applicants are requested to specifically point out to the specification what may represent them. And if they are distinct elements, Applicants

are required to provide essential structural cooperative relationships between them. MPEP 2172.01 clearly states that "a claim which fails to interrelate (emphasis added) essential elements of the invention as defined by applicant(s) in the specification may be rejected under 35 U.S.C. 112, second paragraph, for failure to point out and distinctly claim the invention. See In re Venezia, 530 F.2d 956, 189 USPQ 149 (CCPA 1976); In re Collier, 397 F.2d 1003, 158 USPQ 266 (CCPA 1968)."

The Khosrowpour et al. 102 Rejection:

With regard to claim 1, Applicants argued that Khosrowpour et al. (Khosporowpour) does not disclose or suggest "a slave device that begins to sample a destination address from the bus a plurality of clock cycles after commencement of an address interval." Col. 2, lines 31-41 of Khosrowpour is cited for support. At the outset, it is noted that the prior art reference must be considered in its entirety, i.e. as a whole. In the instant case, Applicants selectively cited and narrowly interpreted only a portion of the prior art reference, and in the process, took it out of context to, at best, try to avoid the prior art reference. In any event, contrary to Applicants' argument, it is clear that in Khosrowpour, the slave device "begin[s] to sample a destination address from the bus a plurality of clock cycles after commencement of an address interval" as recited in claim 1. A clock cycle is the time between two adjacent pulses. The number of these pulses per second defines the clock speed measured in Mhz. In Khosrowpour, each slave device preferably includes a sample circuit for sampling each data bit when the sample circuit is enabled. More particularly, the command logic of each slave

device includes a simple state machine for receiving and properly sequencing through the data and clocking pulses for each data bit. The state machine enables a sample and hold (S/H) or latch circuit when the initial data pulse is asserted. The incorporated data bit is then captured by the sample and hold circuit. A memory device is provided for storing each data bit. Also, control logic detects the data pulse, enables the sample circuit for sampling the data bit, detects the clock pulse to disable the sample circuit and enable the memory, and detects the reset pulse for resetting the slave to receive another data bit. The memory of the slave device is preferably shift memory, which receives the data bits one at a time until filled with the address. Thus, it is clear that a clock cycle is terminated after the S/H sampled one bit and the reset pulse resets another clock cycle for another bit to be sampled. Preferably, the master sends a plurality of data bits forming a command, where each command includes at least one command bit and corresponding address bits. Since the address bits are represented by a plurality of bits, the S/H of the slave must sample the address bits from the bus a plurality of clock cycles. Applicants also argued that "Applicants have reviewed the IC2 bus specification and submit that the specification does not disclose or suggest a slave device that begins to sample a destination address from the bus a plurality of clock cycles after commencement of an address interval." At the outset, it is apparent that this is simply Applicants' own failure to fully understand how the IC2 bus works even after reviewing the I2C bus specification. In any event, it is the Examiner's position that the sampling process of Khosrowpour as explained above is fully in compliance with

I2C bus specification; wherein the S/H of the slave must sample the address bits from the bus a plurality of clock cycles after commencement of an address interval.

With regard to claim 3, Applicants argued that Khosrowpour does not disclose " a data/address interval signal line configured to differentiate the data interval from the address interval." At the outset, it is noted that Applicants have already conceded that Khosrowpour et al., col. 2, lines 11-23, that "the master transmits several data bits implementing a command, where each bit is combined with clocking pulses" and "each command includes at least one command bit and corresponding address bit" (col. 2, lines 32-34). Further, it is clear from Khorowspour that '[o]peration is repeated for each data bit sent until command is retrieved, which includes an initial command bit followed by several address decode bits. Decode logic decodes bits and enables an output flip-flop to receive the command bit as clocked by the final reset pulse. If so enabled, the command is performed" (col. 11, lines 7-12). Still further, it is also true for any I2C bus that all ICs (slaves) monitor the bus to determine if the master device is sending their address. Only the slave device with the correct address communicates with the master in order to receive data. Thus, it is clear that the "data interval" is differentiated from the "address interval." Only slave device having correct/matched address continues to receive data during "data interval." Applicants also argued that "the Examiner has admitted something quite different: 'The I2C Bus physically consists of 2 active wires and a ground connection ... Only two lines (clock and data) are required for full duplexed communication between multiple devices' ... therefore, according to the Examiner the I2C bus does not include a data/address interval signal line." At the

outset, Applicants' rationale cannot be ascertained. While it is not clear to Applicants, it is clear to the Examiner that both address bits and data are transmitted via the same I2C data line (as in both I2C specification and Khosrowpour, Fig. 1A) or the so-called "data/address interval signal line" at differentiated intervals.

With regard to claim 13, in response to Applicants' similar argument presented in the 10/9/2003 amendment, the Examiner stated that "the Examiner provides clear explanation (Office Action, page 2) regarding I2C bus and I2C specification. Reference to Figures 1, 1a, 2, and description thereof were also given to Applicants." It is clear that I2C bus must be fully in compliance with the I2C bus specification. However, the Examiner mistakenly cited the "M_PRESENT" line as an example, instead of the DATA line. However, this, by no means, invalidates the rejection of claim 13, which is based on the protocol set forth in the I2C bus of Khosrowpour which must be in full compliance with the I2C specification. According to the I2C specification, when an address or data byte has been transmitted onto the bus then this must be ACKNOWLEDGED by the slave(s). In case of an address: If the address matches its own then that slave and only that slave will respond to the address with an ACK. In case of a byte transmitted to an already addressed slave then that slave will respond with an ACK as well.

With regard to claim 26, see explanation above. Note also that address bits and data are transmitted during differentiated intervals, and therefore, at differentiated clock cycles.

The Khosrowpour 103 Rejection:

Similar to the argument presented in the 10/9/2003 Amendment, Applicants argued that "the Examiner's 'obvious design choice' argument lacks merit. The Examiner disagrees, and it is still the Examiner's position that selecting a particular number of clock cycles is only a matter of design choice, and involves only routine skill in the art. A clock cycle is the time between two adjacent pulses. The number of these pulses of an oscillator per second defines the clock speed which is measured in Mhz and sets the tempo for, in the instant case, the I2C bus system. Depending on the clock speed, it takes less or more time to complete a data transaction or for data to reach the slave so that it can begins to sample. As a matter of fact, the originally filed specification is virtually silent on the matter of any purported advantage to employ "5 clock cycles" and does not clearly state that the use of "5 clock cycles" solves any particular problem or produces any unexpected result." Indeed, the use of "5 clock cycles" is only disclosed as an example in the originally filed specification, and therefore, clearly a matter of design choice. *In re Rice,* 341 F.2d 309, 144 USPQ 476 (CCPA 1965); In re Kuhle, 526 F.2d 553, 555, 188 USPQ 7, 9 (CCPA 1975). In any event, In any event, it has been held that discovering an optimum value (a particular number of clock cycles) of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

The Dickson et al. 102 rejection:

With regard to claims 1, 17, and 26, the rejection of claims 1, 17, and 26 are hereby withdrawn in view of Applicants' amendments and arguments.

With regard to claims 23, Applicants argued that claim 23 recites features similar to features described above with regard to claim 1 ... and therefore, not anticipated by Dickson et al." Applicants' argument cannot be ascertained, since similar features are certainly not identical features. Arguments regarding claim 1 cannot be used for arguments regarding claim 23 unless the claimed features of in both claims are identical. With regard to claims 23 and 27, Applicants also argued that Dickson et al. does not disclose "redundant buses. Contrary to Applicants' argument, the bus shown in Fig. 1 for providing connection between 17 and 24 via 18, not labeled, perpendicular to bus 20, and bus 20 together define redundant buses. The fact that these buses from two masters are connected to the same slave device is evidence that if one bus fails, the other bus can be used to control the slave device by one of the maters. With regard to claim 29, Applicants argued that Dickson et al. does not disclose the "first master device." Contrary to Applicants' argument, one of a plurality of masters (18) can be a "first master device." These masters 18 monitors and communicate to one another and in case if one master fails, the other master will take over.

The Dickson et al. 103 rejection:

Applicants did not separately argued the 103 rejection of claim 25 over Dickson et al.

Allowable Subject Matter

Claims 2 and are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 21 and 22 are allowable if rewritten or amended to overcome the 35 U.S.C. 112, 2nd paragraph.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication should be directed to Khanh Dang at telephone number 703-308-0211.

Khanh Dang
Primary Examiner